UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,826	03/05/2002	Devereaux C. Chen	0023-0052	4763

44987 7590 06/03/2005		EXAMINER
HARRITY & SNYDER, LLP		ROJAS, MIDYS

ART UNIT	PAPER NUMBER
2189	

HARRITY & SNYDER, LLP
11240 WAPLES MILL ROAD
SUITE 300
FAIRFAX, VA 22030

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/087,826	CHEN ET AL.
	Examiner	Art Unit
	Midys Rojas	2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-9 and 12-25* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12* is/are allowed.

6)☒ Claim(s) *1,2,5,6,8,9 and 13-25* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Applicant's arguments, see page 14, filed on 3/14/05, with respect to the rejection(s)of

claims 14-19 have been fully considered and are persuasive. Therefore, the rejection has been

withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view

of Parks et al. [5,517,671] in view of Bronson et al. [6,065,088] further in view of Umeki et al.

[5,98,354].

Response to Arguments

2.   Applicant's arguments filed 3/14/05, with respect to claims 1-2, 5-6, 8-9, 13, 20-25 have

been fully considered but they are not persuasive.

Regarding Claim 1, Applicant argues that the queues of Bronson are separate queues that

output commands to a second set of different queues. The Examiner would like to point out that

as claimed, the claim recites "queueing areas"; therefore, the multiple queues of the interrupt

routing unit (although they are separate queues) do comprise a first queueing area, and the

multiple remaining queues do comprise a second queueing area.

Additionally, applicant argues that the data in queues 148 and 150 are not parallel.

However, the data is these queues progress through parallel paths, and thus, are parallel.

Finally, in response to applicant's argument that one of ordinary skill in the art would not

be motivated to bypass the interrupt routing unit of Bronson; the Examiner would like to point

out that some commands in the system of Bronson already bypass the queues 134 and 136

[MMIO Commands, see Fig. 3]. Therefore, it would be feasible for the interrupt routing unit 142

to bypass the queues when they are empty since control logic 140 already bypasses these queues.

Regarding Claims 8 and 20, applicant argues that multiplexer 144 teaches away from receiving a plurality of dta items for each cycle of the queue. However, Bronson teaches that for every cycle of the queue 146 and EOI command and a MMIO command is received, yet only one is selected. Therefore, multiple data items are received for each cycle of the queue.

Additionally, in response to applicant's argument that one of ordinary skill in the art would not be motivated to bypass the interrupt routing unit of Bronson; the Examiner would like to point out that some commands in the system of Bronson already bypass the queues 134 and 136 [MMIO Commands, see Fig. 3]. Therefore, it would be feasible for the interrupt routing unit 142 to bypass the queues when they are empty since control logic 140 already bypasses these queues.

Regarding Claim 22, applicant argues that Bronson is completely devoid of any disclosure or suggestion to modify the multiplexer as suggested. However, in Col. 8, lines 42-55, Bronson states that when queue 148 is busy, queue 150 continues to be serviced; therefore, when queue 148 is not busy, both queues are being serviced, giving priority to servicing higher priority queue 150. This implies the need for input arbitration into bus control logic 152. Since Bronson already teaches the use of a multiplexer as an input arbitration solution, a multiplexer could be used here for the same purpose in a manner that would still give higher priority to the servicing of queue 150.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks et al.

[5,517,671] in view of Bronson et al. (6,065,088) further in view of Umeki et al. (5,928,354).

Regarding Claim 14, Parks discloses a request manager configured to receive memory

requests [Fig. 1, system controller 20], a plurality of processors [Processors 1 and 2] configured

to receive the memory request from the request manager, a memory request arbiter configured to

receive the memory request from the plurality of processors, the memory request arbiter [MIC

made up of EISA I/O Bridges in combination with the system controller, see Col. 5, lines 3-11

and Col. 6, lines 38-45] transmitting the memory request to a memory system [peripherals] based

on an arbitration scheme. Park does not disclose the details of the memory request arbiter or

interrupt controller. Bronson discloses an interrupt unit [arbiter, Figure 3] for each processor

[Figure 1] receiving memory commands through system bus [101] where the memory commands

originate from the processor; and queues [see Figure 3] for each processor (since each processor

would have its own interrupt unit) configured to enqueue and dequeue memory requests, and

buffers [148, 150] configured to receive memory request dequeued from the queues when the

queues contain memory requests. It would have been obvious to one of ordinary skill in the art

at the time the invention was made to replace the MIC of Parks with the interrupt unit of Bronson

since Parks does not disclose the details of implementation of its Interrupt Controller and

Bronson's system disclose a form of implementing an Interrupt Unit. These units are

interchangeable.

Although Bronson et al. teaches a buffer or queue receiving memory requests dequeued

from another queue, Parks in view of Bronson does not teach forwarding the data items directly

to a buffer when the queue is empty.   Umeki et al. teaches a bypass logic described in Figure 5A

wherein the receiving queue (instruction queue 2) is bypassed when it is empty (see Column 4,

lines 33-50). It would have been obvious to one of ordinary skill in the art at the time the

invention was made to bypass the queues of Bronson as done by Umeki et al. since doing so

improves access reliability and speed (see Umeki, Column 4, lines 46-50; "reliability to access

memory is improved").

Regarding Claims 15 and 17, Bronson et al. teaches a second queuing area which

includes a normal priority queue 148 and a high priority queue 150 which act as independent

buffers ("first buffer... second buffer"). In addition, Bronson et al. discloses an I/O bus control

logic 152 ("encoding component"), which reads data from the priority queues, giving higher

priority to the high priority queue 150, and passes on the data read to the I/O Bus 102 (Figure 3,

Column 8, lines 20-32).

Regarding Claim 16, Bronson et al. teaches a queuing system with the ability to bypass

the first queuing area by sending specific commands directly to the command queue in the

second queuing area through bus 141 ("bypass logic"). When bypassing interrupt routing unit,

specific commands are being sent that do not need to go through this first queuing area, and thus,

the command queue in the second queuing area should be ready to accept the data that is being

sent through bus 141.

Regarding Claim 18 since the I/O Bus control logic is a controller based mechanism, it is

possible for it to be composed of a controller with the ability to read more than one data item per

clock cycle (Figure 3 and Column 8, lines 20-32).

Regarding Claim 19, Bronson et al. teaches a queuing system for access commands that could be used to arbiter commands from a plurality of local or remote sources or connected units, even in a networking environment, and therefore, could be part of a network router (Column 3, lines 34-44).

5.   Claims 1-2, 5-6, 8-9, 13, and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronson et al. (6,065,088) in view of Umeki et al. (5,928,354).

Regarding Claim 1, Bronson et al. teaches a queuing system divided into two areas,

an interrupt routing unit ("first queuing area") divided into two parallel queues, the EOI queue 136 and the INR, IRR queue 134 ("plurality of parallel sub-queues", Figure 3)

and the remaining queues ("second queuing area") which include a normal priority queue 148 and a high priority queue 150 which act as independent buffers ("first buffer... second buffer").

In this system, the second queuing area has the ability to receive data from the first queuing area through buses 137 and 139 (see Figure 3). The queuing system of Bronson et al. does not teach bypassing the first queuing area and sending commands directly to the second queuing area. Umeki et al. teaches a bypass logic described in Figure 5A wherein the first queuing area (instruction queue 2) is bypassed when it is empty (see Column 4, lines 33-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to bypass the first queuing area of Bronson et al. as done by Umeki et al. since doing so improves access reliability and speed (see Umeki, Column 4, lines 46-50; "reliability to access memory is improved").

Regarding Claims 8 and 20, Bronson et al. teaches a FIFO command queue 146 receiving

memory mapped input/output (MMIO) commands from a system bus control logic 140and EOI

commands from EOI Output queue 136 ["a plurality of data items for each cycle of the queue"].

When the command queue is not empty, new data items are simply added to the top of the queue

["enqueuing"] as older data items are de-queued and transferred to the normal priority queue via

bus 147 ["enqueuing... dequeuing..."]. These items pass to a second queuing area, of which the

normal priority queue is part of, which includes a normal priority queue 148 and a high priority

queue 150 which act as independent buffers ("first buffer... second buffer"). In addition,

Bronson et al. discloses an I/O bus control logic 152 ("encoding component"), which reads data

from the priority queues, giving higher priority to the high priority queue 150, and passes on the

data read to the I/O Bus 102 (Figure 3, Column 8, lines 20-32). Once an item is sitting in the

normal priority queue 148, it will eventually be outputted through the I/O Bus Control logic 152

and I/O bus 102 (see Figure 3, column 8, lines 33-41). In this instance, the normal priority

queue acts as a buffer receiving the de-queued data items prior to the transmission. Bronson et

al. does not teach forwarding the data items to a buffer when the queue is empty. Umeki et al.

teaches a bypass logic described in Figure 5A wherein the receiving queue (instruction queue 2)

is bypassed when it is empty (see Column 4, lines 33-50). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to bypass the first queuing area of

Bronson et al. as done by Umeki et al. since doing so improves access reliability and speed (see

Umeki, Column 4, lines 46-50; "reliability to access memory is improved").

Regarding Claims 2, 9, and 21, Bronson et al. teaches the queuing to memory mapped

input/output (MMIO) commands as well as memory interrupt commands. These commands

affect the access of a memory, therefore, they can be considered to be a type of memory access command (Abstract and Figure 3).

Regarding Claim 5, Bronson et al. teaches a second queuing area which includes a normal priority queue 148 and a high priority queue 150 which act as independent buffers ("first buffer... second buffer"). In addition, Bronson et al. discloses an I/O bus control logic 152 ("encoding component"), which reads data from the priority queues, giving higher priority to the high priority queue 150, and passes on the data read to the I/O Bus 102 (Figure 3, Column 8, lines 20-32).

Regarding Claims 6, and 13, since the I/O Bus control logic is a controller based mechanism, it is possible for it to be composed of a controller with the ability to read more than one data item per clock cycle (Figure 3 and Column 8, lines 20-32).

2.   Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronson et al. (6,065,088).

Regarding Claim 22, Bronson et al. teaches the arbiter of figure 3, which arbiters access commands through the use of multiple queues. Each queue of the arbiter, specifically the command queue 146, queue items at the beginning of the queue ("first stage") and de-queue items at the end of the queue ("last stage") due to their FIFO structure. In addition, the arbiter of figure 3 includes a plurality of queuing areas, of which the second queuing area includes a normal priority queue 148 and a high priority queue 150 which act as independent buffers ("first buffer... second buffer"). Bronson et al. also discloses an I/O bus control logic 152 ("arbitration logic"), which reads data from the priority queues, giving higher priority to the high priority queue 150, and passes on the data read to the I/O Bus 102 (Figure 3, Column 8, lines 20-32).

Bronson does not teach the use of a multiplexor connected to multiple stages of a queue,

outputting selected data items, and coupled to and controlled by the I/O bus control logic 152. It

would have been obvious to one of ordinary skill in the art to add a multiplexor between buses

149, 151 and the I/O control logic 152 since multiplexors are shown to be used in the selection of

signals as in Figure 3, reference #144 and such a component would be useful in selecting signals

from either bus 149 or bus 151 (Figure 3). In adding such multiplexor, it would be connected to

the ends of two output queues, however, since in a queue each stage of the queue is connected to

the next stage of the queue, essentially the multiplexor would be connected to all stages of the

queues.

In Col. 8, lines 42-55, Bronson states that when queue 148 is busy, queue 150 continues

to be serviced; therefore, when queue 148 is not busy, both queues are being serviced, giving

priority to servicing higher priority queue 150. This implies the need for input arbitration into

bus control logic 152. Since Bronson already teaches the use of a multiplexer as an input

arbitration solution, a multiplexer could be used here for the same purpose in a manner that

would still give higher priority to the servicing of queue 150.

Regarding Claim 23, Bronson et al. teaches a queuing system with the ability to bypass

the first queuing area by sending specific commands directly to the command queue in the

second queuing area through bus 141 ("bypass logic"). It is understood that when bypassing

interrupt routing unit, specific commands are being sent that do not need to go through this first

queuing area, and thus, the command queue in the second queuing area should be ready to accept

the data that is being sent through bus 141.

Regarding Claim 24, Bronson et al. teaches the queuing to memory mapped input/output

(MMIO) commands as well as memory interrupt commands. It is understood that since these

commands affect the access of a memory, they can be considered to be a type of memory access

command (Abstract and Figure 3).

Regarding Claim 25, Bronson et al. discloses a queuing system in which the command

queue is implemented as a FIFO queue (Column 8, lines 33-36).

Allowable Subject Matter

6.   Claim 12 is allowed.

The Prior Art of Record does not teach moving data from a second low priority buffer to

a first high priority buffer when such high priority buffer is free to receive new items. Bronson

et al. (6,065,088) teaches outputting data from the low priority output queue 148 through bus 149

only when the high priority queue 150 has been emptied through bus 151. The data in the low

priority queue 148 is never moved to the high priority queue 150 (Figure 3).

7.   Claim 7 is objected to as being dependent upon a rejected base claim, but would be

allowable if rewritten in independent form including all of the limitations of the base claim and

any intervening claims.

The Prior Art of Record does not teach masking logic coupled to output buffers and

configured to restore requests that were not read from the output buffers in combination with a

queue system divided in to multiple queuing areas of which the second area contains two output

priority buffers.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The

examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 27, 2005

Midys Rojas

Midys Rojas
Examiner
Art Unit 2189

MI

Mano Padmanabhan 5/31/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER